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| 09/031,326 | 02/26/1998 | JOSEPH J. KARNIEWICZ | 303.376US1 | 8474 |

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| EXAMINER | |
|---|---|
| PHAN, THAI Q | |

| ART UNIT | PAPER NUMBER |
|---|---|
| 2123 | |

DATE MAILED: 10/04/2002

Please find below and/or attached an Office communication concerning this application or proceeding.



PRH

| Office Action Summary | Application No. 09/031,326 | Applicant(s) Joseph J. Karniewicz |
|---|---|---|
| | Examiner Thai Phan | Art Unit 2123 |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136 (a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1) ☒ Responsive to communication(s) filed on *Jul 31, 2002* .

2a) ☐ This action is **FINAL.** 2b) ☒ This action is non-final.

3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11; 453 O.G. 213.

**Disposition of Claims**

4) ☒ Claim(s) *1-25* is/are pending in the application.

4a) Of the above, claim(s) _____ is/are withdrawn from consideration.

5) ☐ Claim(s) _____ is/are allowed.

6) ☒ Claim(s) *1-25* is/are rejected.

7) ☐ Claim(s) _____ is/are objected to.

8) ☐ Claims _____ are subject to restriction and/or election requirement.

**Application Papers**

9) ☐ The specification is objected to by the Examiner.

10) ☐ The drawing(s) filed on _____ is/are a) ☐ accepted or b) ☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11) ☐ The proposed drawing correction filed on _____ is: a) ☐ approved b) ☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12) ☐ The oath or declaration is objected to by the Examiner.

**Priority under 35 U.S.C. §§ 119 and 120**

13) ☐ Acknowledgement is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a) ☐ All b) ☐ Some* c) ☐ None of:

1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

*See the attached detailed Office action for a list of the certified copies not received.

14) ☐ Acknowledgement is made of a claim for domestic priority under 35 U.S.C. § 119(e).

a) ☐ The translation of the foreign language provisional application has been received.

15) ☐ Acknowledgement is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s). _____
4) ☐ Interview Summary (PTO-413) Paper No(s). _____
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other:

## DETAILED ACTION

This Office Action is response to a CPA of the related patent application, filed July 31, 2002. Claims 1-25 are pending in this official action.

### *Claim Rejections - 35 USC § 103*

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1-25 are rejected under 35 U.S.C. 103(a) as being unpatentable over Robinson et al., patent no. 5,524,244 in view of Ho, patent no. 6,421,814 B1.

As per claims 1 and 9, Robinson discloses method, design system with databases stored in memory, program product for populating parameters of cells or design configuration files (Abstract,"Summary of the Invention", col. 3, line 65 to col. 5, line 30) for use in circuit design environment and realization of silicon on chip design substantially similar to the claimed invention. According to Robinson, the design apparatus includes global files for global variables and design data relating to layout or schematics layout and connectivity data of the functional block, a plurality of cell configuration files or claimed local files, each relating a plurality of local variables to the global variables in system files (col. 6, lines 21-36, col. 8, lines 41-67, col. 9, lines 1-12), and a plurality of cells, each cell corresponding to a local file and having a set of

parameters derived by relating the local variables to the global variables in the global source files such that the changes of global variables in the global files reflect or may cause changes in the programmable cells (Figs. 3-12, col. 34, "Overview", col. 35, lines 1-28, col. 36, line 55 to col. 37, line 17, col. 53, lines 44-55, cols. 50-56, 59-62 for example). Robinson does not expressly disclose geometric variables related to physical layout in hierarchical manner as claimed. Such feature limitation is well-known in the art. Ho teaches geometrical layout variables or parameters and such relations in geometry layout data for physical design with faster and better layout in integrated circuit design (Background of the Invention, col. 1, lines 48-60, Fig. 1B, col. 5, lines 33-60).

This would motivate practitioner in the art at the time of the invention was made to use Ho teaching of geometrical layout variables in hierarchical relationships for physical design of the integrated circuit as disclosed in Robinson to better improve and faster layout processing in circuit complexity as in Robinson design.

As per claims 2-3 and 10-11, Robinson disclosed local files include inherent file from source files, instance files, data files, etc. (Figs. 3-12).

As per claim 4, Robinson disclosed master files in hierarchical design acting as initial version of a corresponding local file for design, modification, increment compilation, etc.

As per claim 5, Robinson disclosed file or clean sheet file for containing design rules for a plurality of cells for coordinated design as claimed.

As per claim 6, Robinson discloses file extraction and related variable extraction for design and update design.

As per claims 7-8, Robinson discloses the design display in local host for display interactively interface.

As per claim 12, Robinson discloses file update including update global file for coordinate process.

As per claim 13, Robinson discloses local display in local user workstation for the design process.

As per claim 14, Robinson discloses computer program in concurrent with design program for circuit design process as claimed.

As per claim 15, Robinson discloses method and system of workstations, databases, shared memory, etc. for populating parameters of cells (Abstract, Figs. 3-12, cols. 4-5, 59-62, for example) for use in circuit design, programming design, silicon on chip design etc. environment similar to the claimed invention. According to Robinson, the design apparatus includes local user work stations, central workstations, global files of global variables and design database, system memory for sharing between users for distribution processing (cols. 4, 5, col. 9, lines 12-23), a plurality of local files, each relating a plurality of local variables to the global variables (cols. 4-5, col. 35, lines 1-28, cols. 50-56, 60-64, for example), and a plurality of instance cells being programmable, each cell corresponding to a local file of subcircuit blocks and having a set of parameters derived by relating the local variables to the global variables in the global source files such that the changes of global variables in the global files reflect or may cause changes in the cells (Figs. 3-12, cols. 4-5, cols. 34-36 for overviews for design methodology, col. 53, lines 44-55, col. 54-56, 60-64, etc.) or updating variables in configuration files or local files by reading

from the global file value of global variables to which the local variables of the local file correspond for complete design as claimed. Robinson does not expressly disclose geometric variables related to physical layout in hierarchical manner as claimed. Such feature limitation is well-known in the art. Ho teaches geometrical layout variables or parameters and such relations in geometry layout data for physical design with faster and better layout in integrated circuit design (Background of the Invention, col. 1, lines 48-60, Fig. 1B, col. 5, lines 33-60).

This would motivate practitioner in the art at the time of the invention was made to use Ho teaching of geometrical layout variables in hierarchical relationships for physical design of the integrated circuit as disclosed in Robinson to better improve and faster layout processing in circuit complex as in Robinson.

Similarly, claims 16-21 are also rejected due to its similarities to claims 2-8 and claims 11-14.

As per claim 22, Robinson discloses method, design system with databases stored in memory, program product for populating parameters of cells (Abstract,"Summary of the Invention", col. 3, line 65 to col. 5, line 30) for use in circuit design environment substantially similar to the claimed invention. According to Robinson, the design apparatus includes global files for global variables and design data relating to layout and connectivity data of the functional block, a plurality of local files, each relating a plurality of local variables to the global variables (col. 6, lines 21-36, col. 8, lines 41-67, col. 9, lines 1-12, col. 34, "Overview", col. 35, lines 1-28, cols. 50-56, 60-64, etc.), and a plurality of cells, each cell corresponding to a configuration file or a local file and having a set of parameters derived by relating the local variables to the global

variables in the global source files such that the changes of global variables in the global files reflect or may cause changes in the programmable cells (Figs. 3-12, cols. 59-62 for example). Robinson does not expressly disclose geometric variables related to physical layout in hierarchical manner as claimed. Such feature limitation is well-known in the art. Ho teaches geometrical layout variables or parameters and such relations in geometry layout data for physical design with faster and better layout in integrated circuit design (Background of the Invention, col. 1, lines 48-60, Fig. 1B, col. 5, lines 33-60).

This would motivate practitioner in the art at the time of the invention was made to use Ho teaching of geometrical layout variables in hierarchical relationships for physical design of the integrated circuit as disclosed in Robinson to better improve and faster layout processing in circuit complex as in Robinson.

As per claims 23-24, Robinson discloses inherent design file, and instance file in the design database.

As per claim 25, Robinson discloses design framework for use in the chip design process. Such design framework could be used as CADENCE functional design system as claimed.

***Response to Arguments***

3. Applicant's arguments filed July 31, 2002 have been fully considered but they are moot in view of a new ground of rejection.

In response to applicant's argument Robinson does not teach geometric variables relating to a physical layout of element blocks (page 3, last paragraph to page 4, paragraph 1), the

examiner agrees with. Such argued feature limitation is however well-known in the art. In fact, Ho teaches geometrical layout variables or parameters and such relations in geometry layout data for physical design with faster and better layout in integrated circuit design (Background of the Invention, col. 1, lines 48-60, Fig. 1B, col. 5, lines 33-60).

This would motivate practitioner in the art at the time of the invention was made to use Ho teaching of geometrical layout variables in hierarchical relationships for physical design of the integrated circuit as disclosed in Robinson to improve better and faster layout processing in circuit complexity as in Robinson.

***Conclusion***

*4.* The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

1. Patent no. 6,425,113 B1, issued to Anderson et al., July 2002

5. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thai Phan whose telephone number is (703) 305-3812.

Any inquiry of a general nature or relating to the status of this application should be directed to the Group receptionist whose telephone number is (703)305-3900.

Any inquiry of a general nature or relating to the status of this application should be directed to the Group receptionist whose telephone number is (703)305-3900.

**Any response to this action should be mailed to:**

Commissioner of Patents and Trademarks

Washington, D.C. 20231

**or faxed to:**

(703) 746-7239, (for formal communications intended for entry)

**Or:**

(703) 746-7240 (for informal or draft communications, please label "PROPOSED" or "DRAFT")

Hand-delivered responses should be brought to Crystal Park II, 2121 Crystal Drive, Arlington. VA., Sixth Floor (Receptionist).

September 22, 2002

KEVIN J. TESKA
SUPERVISORY
PATENT EXAMINER